

**Amendments to the Claims**

This listing of claims, if entered, will replace all prior versions and listings of claims in the above-identified application.

**Listing of Claims**

- 1-27. Cancelled
28. (Previously Presented) A method comprising:  
issuing an instruction to transfer data between a memory and a processor via a  
memory bus, wherein the data comprises a plurality of data elements each  
having a data width, wherein the data width of the data elements is less  
than a width of the memory bus, and wherein the plurality of data  
elements are stored in non-contiguous locations in the memory;  
packing two or more of the data elements of the plurality into a data block;  
transferring the data block between the memory and the processor via the memory  
bus coupled therebetween so that the two or more data elements are  
transferred at a time.
29. (Previously Presented) The method of claim 28 further comprising:  
determining an ending address of the data to be transferred from a starting address  
contained in the instruction and the data width;  
generating an address exception when it is determined that the data to be  
transferred crosses a page boundary of a page in the memory.

30. (Previously Presented) The method of claim 29 wherein:  
the instruction comprises a length of the data to be transferred and a stride of the  
data to be transferred;  
wherein determining the ending address comprises:  
multiplying the stride and the data width to provide a first result;  
subtracting one from the length to provide a second result;  
multiplying the first result and the second result to provide a third result; and  
adding the third result to the starting address to provide the ending address.
31. (Previously Presented) The method of claim 28 further comprising:  
transferring the data to be transferred between the memory and the processor via a  
burst transfer.
32. (Previously Presented) The method of claim 29 further comprising:  
interrupting the data transfer in response to generating the address exception.
33. (**Currently Amended**) A ~~computer readable medium~~ magnetic storage media  
comprising instructions executable by a computer system, wherein the computer system  
performs a method in response to executing the instructions, the method comprising:  
determining a quantity of data elements to be transferred in parallel between a  
memory and a processor via a memory bus coupled therebetween, wherein  
the quantity is determined from a width of the data elements to be  
transferred and a width of the memory bus, wherein the width of each of  
the data elements is less than the width of the memory bus, and wherein  
the data elements are stored in non-contiguous locations in the memory;  
packing the quantity of data elements into a data block;  
initiating a transfer of the data block between the memory and the processor so  
that the quantity of data elements are transferred in parallel.

34. **(Currently Amended)** The ~~computer readable medium~~ magnetic storage media of claim 33 wherein the method further comprises:

determining an ending address of data to be transferred between the memory and the processor via the memory bus, wherein the data includes the quantity of data elements, wherein the ending address is determined from a starting address of the data and the width of the data elements;  
generating an address exception when it is determined that the data to be transferred crosses a page boundary of a page in the memory.

35. **(Currently Amended)** The ~~computer readable medium~~ magnetic storage media of claim 34 wherein determining the ending address comprises:

multiplying a stride of the data to be transferred and the width of the data elements to provide a first result;  
subtracting one from a length of the data to be transferred to provide a second result;  
multiplying the first result and the second result to provide a third result; and adding the third result to the starting address to provide the ending address.

36. **(Currently Amended)** The ~~computer readable medium~~ magnetic storage media of claim 34 wherein the method further comprises:

transferring the data to be transferred between the memory and the processor via a burst transfer.

37. **(Currently Amended)** The ~~computer readable medium~~ magnetic storage media of claim 34 wherein the method further comprises:

interrupting the data transfer in response to generating the address exception.

38. **(Currently Amended)** The ~~computer readable medium~~ magnetic storage media of claim 37 wherein the method further comprises:

performing a burst transfer of the stream of data from the memory to the buffer of the processor, the burst transfer bypassing a data cache of the processor.

39. (Previously Presented) An apparatus comprising:

- a memory;
- a processor coupled to the memory;
- a circuit coupled to the processor, wherein the circuit is configured to calculate a quantity of data elements to be transferred between the memory and the processor via a memory bus coupled therebetween, wherein the circuit calculates the quantity from a width of the data elements and a width of the memory bus, wherein the width of each of the data elements is less than the width of the memory bus, wherein the data elements are stored in non-contiguous locations in the memory, wherein the circuit is configured to pack the quantity of data elements into a data block, and wherein the data block is configured for transmission over the memory bus so that the quantity of data elements are transferred at the same time.

40. (Previously Presented) The apparatus of claim 39 wherein the circuit is configured to generate an ending address of data to be transferred between the memory and the processor via the memory bus, wherein the circuit generates the ending address from a starting address of the data to be transferred and the data width of the data elements, wherein the data includes the data elements, and wherein the circuit generates an address exception when it is determined that the data to be transferred crosses a page boundary of a page in the memory.

41. (Previously Presented) The apparatus of claim 40 wherein the circuit generate data width to provide a first result;

- subtracting one from a length of the data to be transferred to provide a second result;
- multiplying the first result and the second result to provide a third result; and
- adding the third result to the starting address to provide the ending address.

42. (Previously Presented) The method of claim 28, wherein said transferring comprises: transferring said data to a register of the processor.